



## Firmware Control sheet

	<b>Drg</b>	<b>15.4 Sniffer.hex</b>	
	<b>Description</b>		
<b>Issue</b>	<b>ECN</b>	<b>Date</b>	<b>Reason for Change</b>
<b>1</b>	<b>n/a</b>		<b>First Issue</b>

<b>Device</b>	<b>18LF4550</b>
<b>R.F. Sols. ref.</b>	

Design Requirements		
Feature	(Default)	Design / Customer Requirement
Ident. Mark	<i>Dot</i>	
Oscillator		INT RC, RA6, RA7 ports
Fail safe clock mon		Disabled
Oscillator Switch Enable		Disabled
Power Up Timer		Disabled
B.O.D.		Disabled
B.O.Voltage.		2.0V
Watchdog		Disabled,
Watchdog Postscaler		1:512
CCP2 Mux		RB3
Port B A/D Enable		Digital I/O on reset
Low power timer 1		Disabled
Master Clear Enable		RB3 input Enabled
Stack Overflow Reset		Enabled
LV Program		Disabled
Code Protect		All disabled (not code protected)
Data EE Protect		Disabled
Read protect		All Disabled
Write protect		All Disabled
B'gnd. debug		Disabled

Serialisation?		<b>No</b>	
Type		<b>Random</b>	
Start Address		<b>\$</b>	
No of Words		<b>decimal -</b>	

<b>Checksum</b>	<b>0x2F08</b>
-----------------	---------------

<b>Other Requirements</b>	
---------------------------	--